

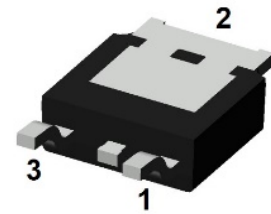
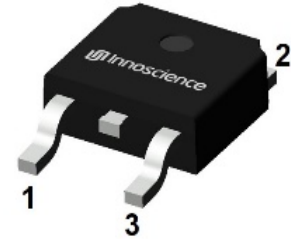
INN700TK240C

1. General description

700V GaN-on-Silicon Enhancement-mode Power Transistor in TO-252 package.

2. Features

- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant



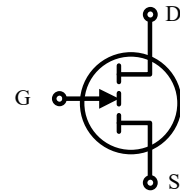
3. Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High density power conversion
- High efficiency power conversion

4. Key performance parameters

Table 1 Key performance parameters at $T_j = 25\text{ }^\circ\text{C}$

Parameter	Value	Unit
$V_{DS,max}$	700	V
$R_{DS(on),max}$ @ $V_{GS} = 6\text{ V}$	240	m Ω
$Q_{G,typ}$ @ $V_{DS} = 400\text{ V}$	2	nC
$I_{D,pulse}$	18	A
Q_{OSS} @ $V_{DS} = 400\text{ V}$	21	nC
Q_{rr} @ $V_{DS} = 400\text{ V}$	0	nC



5. Pin information

Table 2 Pin information

Gate	Source	Drain
1	2	3

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN700TK240C	TO-252	70TK240C

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6. Maximum ratings

at $T_j = 25\text{ °C}$ unless otherwise specified.

Exceeding the maximum ratings may destroy the device. For further information, contact Innoscence sales office.

Table 4 Maximum ratings

Parameter	Symbol	Values	Unit	Note/Test Condition
Drain source voltage	$V_{DS, max}$	700	V	$V_{GS} = 0\text{ V}$; $T_j = -55\text{ °C}$ to 150 °C
Drain source voltage transient ¹	$V_{DS, transient}$	800	V	$V_{GS} = 0\text{ V}$
Drain source voltage, pulsed ²	$V_{DS, pulse}$	750	V	$T_j = 25\text{ °C}$; total time < 10 h
				$T_j = 125\text{ °C}$; total time < 1 h
Continuous current, drain source	I_D	10	A	$T_c = 25\text{ °C}$
Pulsed current, drain source ³	$I_{D, pulse}$	18	A	$T_c = 25\text{ °C}$; $V_{GS} = 6\text{ V}$; $t_{PULSE} = 10\text{ }\mu\text{s}$
Pulsed current, drain source ³	$I_{D, pulse}$	10	A	$T_c = 125\text{ °C}$; $V_{GS} = 6\text{ V}$; $t_{PULSE} = 10\text{ }\mu\text{s}$
Gate source voltage, continuous	V_{GS}	-6 to +7	V	$T_j = -55\text{ °C}$ to 150 °C
Gate source voltage, pulsed	$V_{GS, pulse}$	-20 to +10	V	$T_j = -55\text{ °C}$ to 150 °C ; $t_{PULSE} = 50\text{ ns}$, $f = 100\text{ kHz}$; open drain
Power dissipation	P_{tot}	77	W	$T_c = 25\text{ °C}$
Operating temperature	T_j	-55 to +150	°C	
Storage temperature	T_{stg}	-55 to +150	°C	

1. $V_{DS, transient}$ is intended for non-repetitive events, $t_{PULSE} < 200\text{ }\mu\text{s}$.

2. $V_{DS, pulse}$ is intended for repetitive pulse, $t_{PULSE} < 100\text{ ns}$.

3. Limit was extracted from characterization test, not measured during production.

7. Thermal characteristics

Table 5 Thermal characteristics

Parameter	Symbol	Values	Unit	Note/Test Condition
Thermal resistance, junction-ambient	R_{thJA}^1	55	°C/W	
Thermal resistance, junction-case	R_{thJC}	1.62	°C/W	
Maximum reflow soldering temperature	T_{sold}	260	°C	MSL3

1. R_{thJA} is determined with the device mounted on one square inch of copper pad, single layer 2oz copper on FR4 board.

8. Electric characteristics

at $T_j = 25\text{ °C}$, unless specified otherwise

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	1.7	2.5	V	$I_D = 11\text{ mA}; V_{DS} = V_{GS}; T_j = 25\text{ °C}$
		-	1.7	-		$I_D = 11\text{ mA}; V_{DS} = V_{GS}; T_j = 150\text{ °C}$
Drain-source leakage current	I_{DSS}	-	0.4	20	μA	$V_{DS} = 700\text{ V}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C}$
		-	5	-		$V_{DS} = 700\text{ V}; V_{GS} = 0\text{ V}; T_j = 150\text{ °C}$
Gate-source leakage current	I_{GSS}	-	50	-	μA	$V_{GS} = 6\text{ V}; V_{DS} = 0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	165	240	m Ω	$V_{GS} = 6\text{ V}; I_D = 3\text{ A}; T_j = 25\text{ °C}$
		-	360	-		$V_{GS} = 6\text{ V}; I_D = 3\text{ A}; T_j = 150\text{ °C}$
Gate resistance	R_G	-	6	-	Ω	$f = 5\text{ MHz}; \text{open drain}$

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	79	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 400\text{ V}; f = 100\text{ kHz}$
Output capacitance	C_{oss}	-	25	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 400\text{ V}; f = 100\text{ kHz}$
Reverse transfer capacitance	C_{rss}	-	0.2	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 400\text{ V}; f = 100\text{ kHz}$
Effective output capacitance, energy related ¹	$C_{o(er)}$	-	36	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 0\text{ to }400\text{ V}$
Effective output capacitance, time related ²	$C_{o(tr)}$	-	52	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 0\text{ to }400\text{ V}$
Output charge	Q_{oss}	-	21	-	nC	$V_{GS} = 0\text{ V}; V_{DS} = 0\text{ to }400\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	2	-	ns	$V_{DS} = 400\text{ V}; I_D = 6\text{ A}; L = 318\text{ }\mu\text{H};$ $V_{GS} = 6\text{ V}; R_{on} = 10\text{ }\Omega; R_{off} = 2\text{ }\Omega;$ See Figure 22
Turn-off delay time	$t_{d(off)}$	-	4	-	ns	
Rise time	t_r	-	5	-	ns	
Fall time	t_f	-	6	-	ns	

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V.

2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V.

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	2	-	nC	$V_{GS} = 0$ to 6 V; $V_{DS} = 400$ V; $I_D = 3$ A
Gate-source charge	Q_{GS}	-	0.2	-	nC	
Gate-drain charge	Q_{GD}	-	0.7	-	nC	
Gate Plateau Voltage	V_{Plat}	-	2.5	-	V	$V_{DS} = 400$ V; $I_D = 3$ A

Table 9 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	2.6	-	V	$V_{GS} = 0$ V; $I_S = 3$ A
Pulsed current, reverse	$I_{S, pulse}$	-	-	18	A	$V_{GS} = 6$ V; $t_{PULSE} = 10$ μ s
Reverse recovery charge	Q_{rr}	-	0	-	nC	$I_S = 3$ A; $V_{DS} = 400$ V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

9. Electric characteristics diagrams

at $T_j = 25\text{ }^\circ\text{C}$, unless specified otherwise

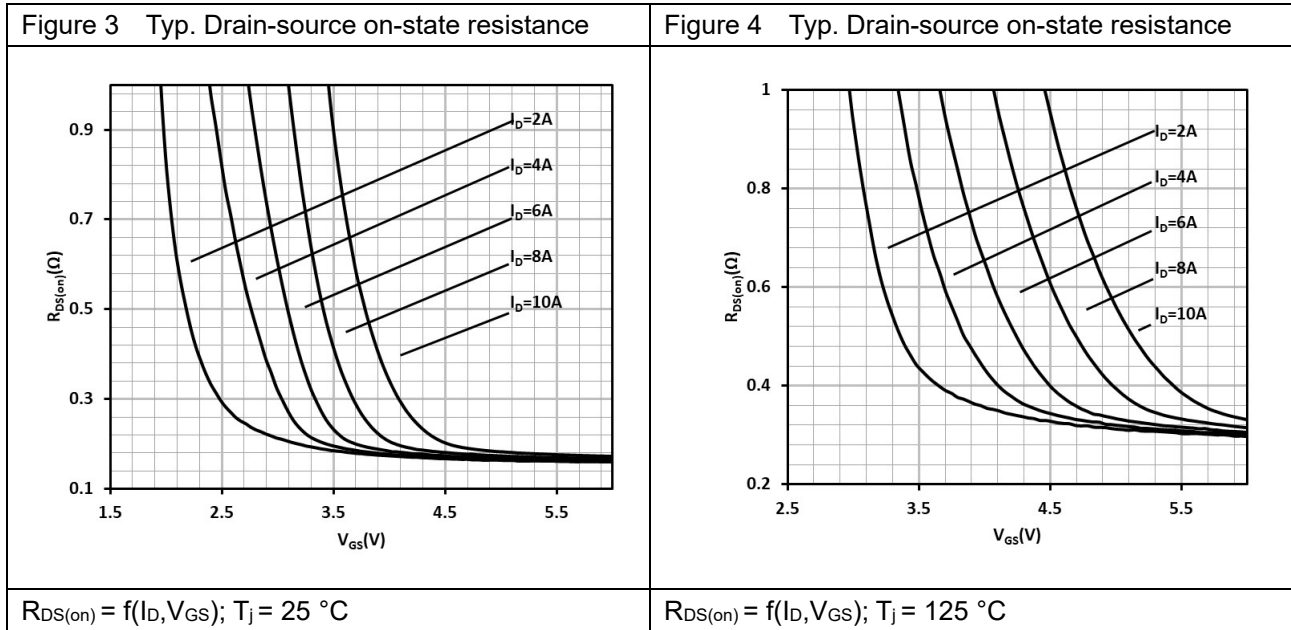
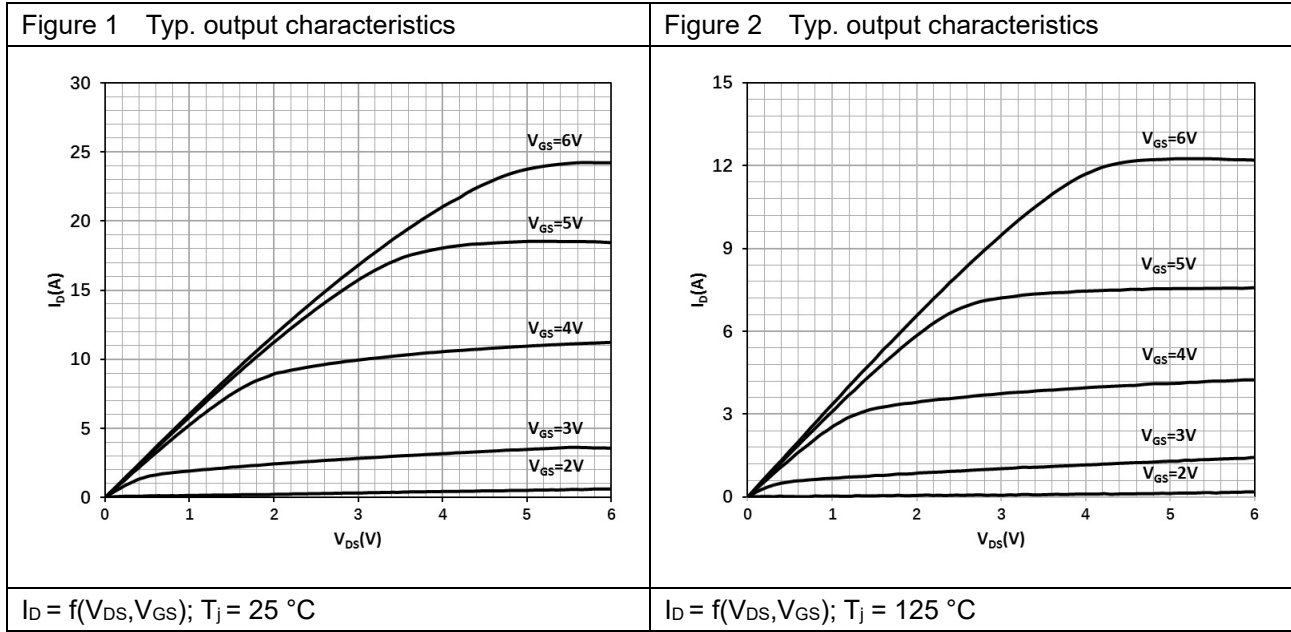
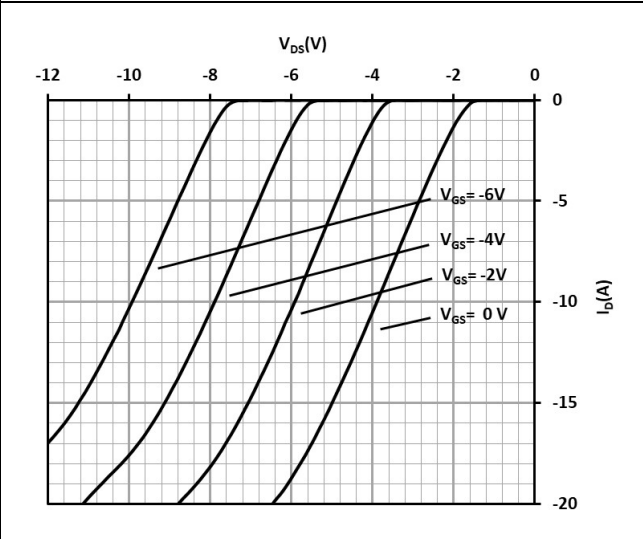
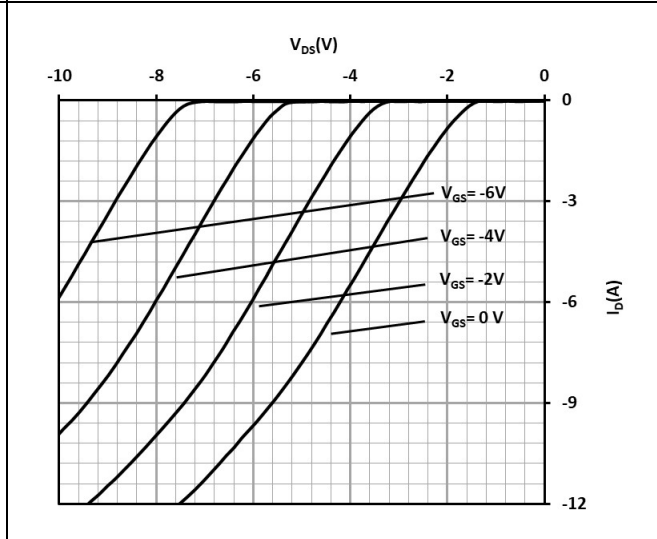


Figure 5 Typ. channel reverse characteristics



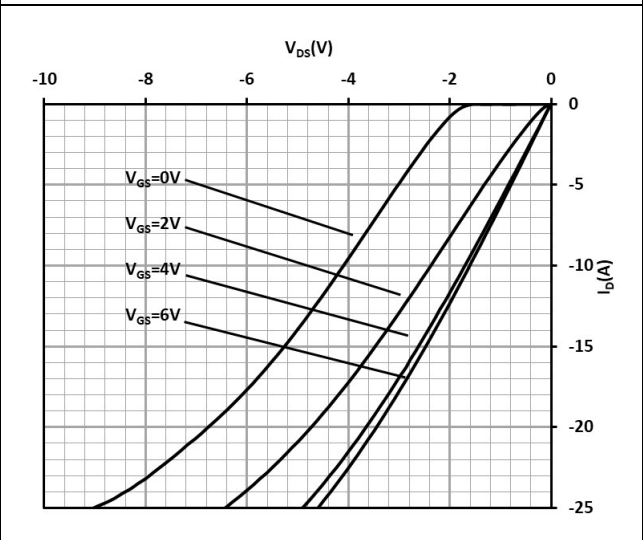
$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ °C}$

Figure 6 Typ. channel reverse characteristics



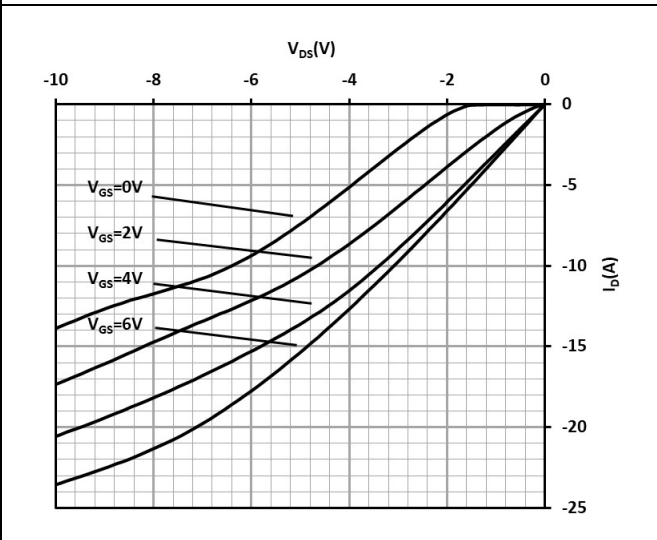
$I_D = f(V_{DS}, V_{GS}); T_j = 125\text{ °C}$

Figure 7 Typ. channel reverse characteristics



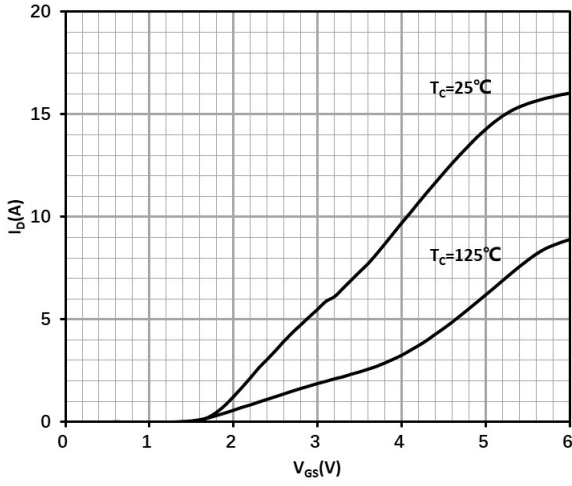
$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ °C}$

Figure 8 Typ. channel reverse characteristics



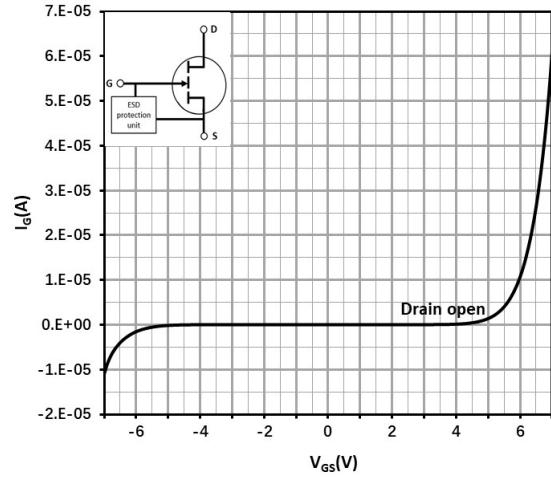
$I_D = f(V_{DS}, V_{GS}); T_j = 125\text{ °C}$

Figure 9 Typ. transfer characteristics



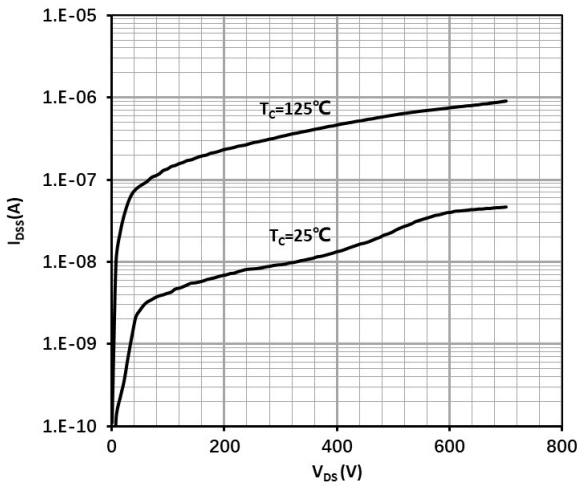
$I_D = f(V_{GS}); V_{DS} = 3\text{ V}$

Figure 10 Typ. Gate-to-Source leakage



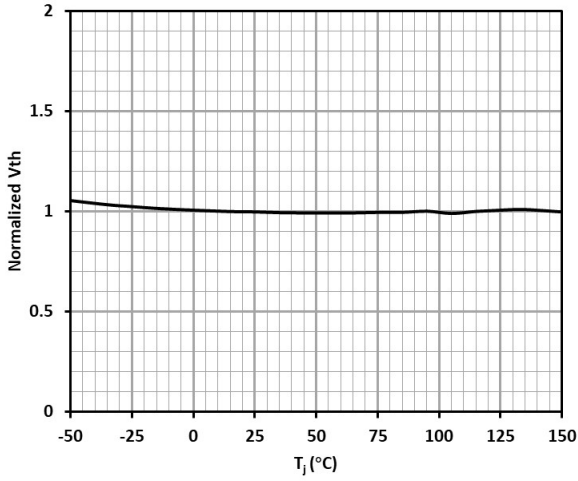
$I_G = f(V_{GS});$

Figure 11 Drain-source leakage characteristics



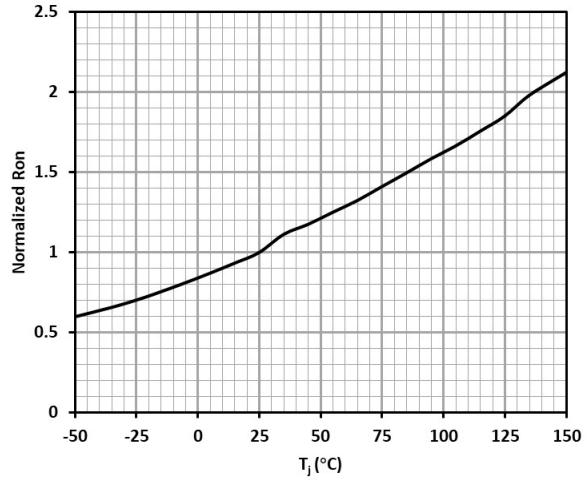
$I_{DSS} = f(V_{DS}); V_{GS} = 0\text{ V}$

Figure 12 Gate threshold voltage



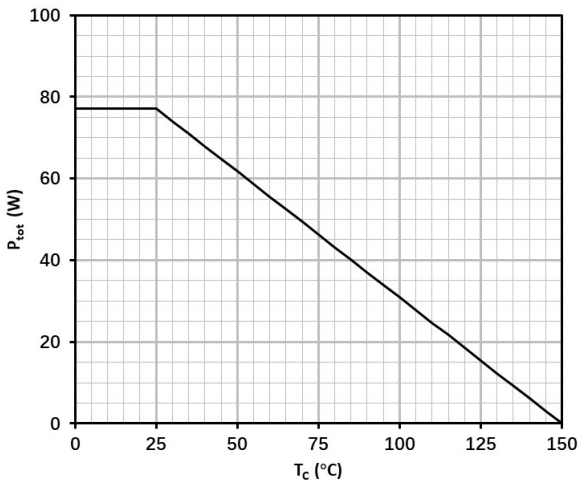
$V_{TH} = f(T_j); V_{GS} = V_{DS}; I_D = 11 \text{ mA}$

Figure 13 Drain-source on-state resistance



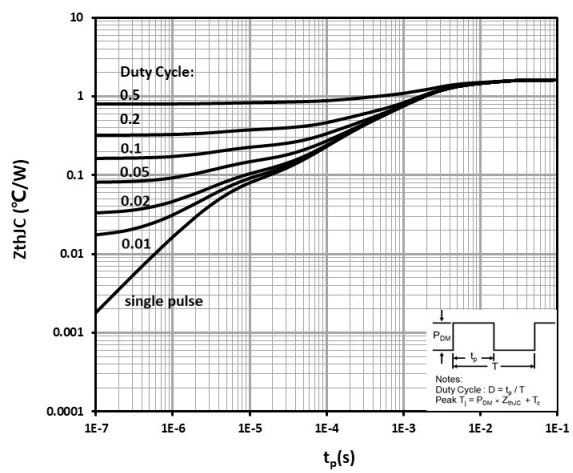
$R_{DS(on)} = f(T_j); I_D = 3 \text{ A}; V_{GS} = 6 \text{ V}$

Figure 14 Power dissipation



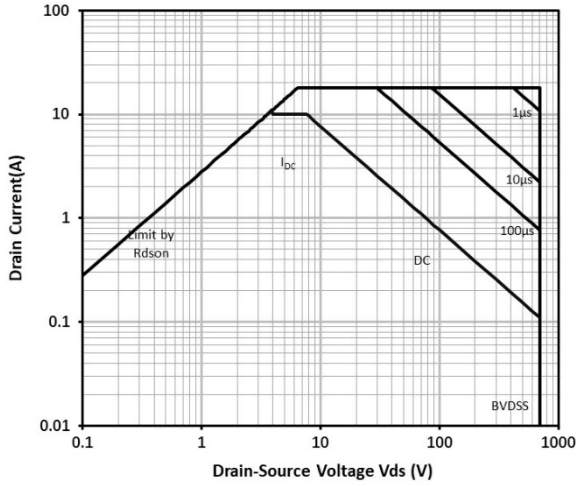
$P_{tot} = f(T_c)$

Figure 15 Max.transient thermal impedance



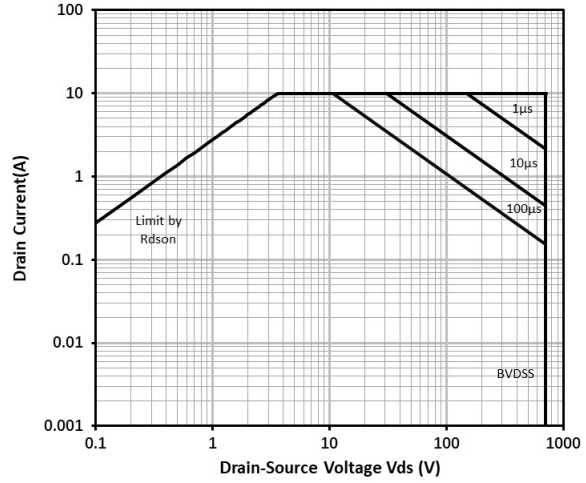
$Z_{thJC} = f(t_p, D)$

Figure 16 Safe operating area



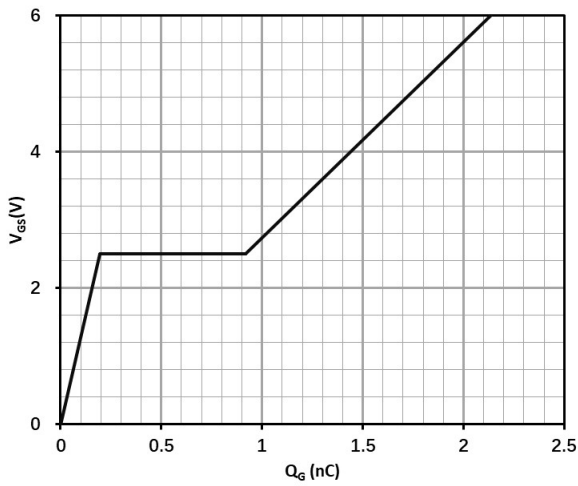
$I_D = f(V_{DS}); T_C = 25\text{ }^\circ\text{C}$

Figure 17 Safe operating area



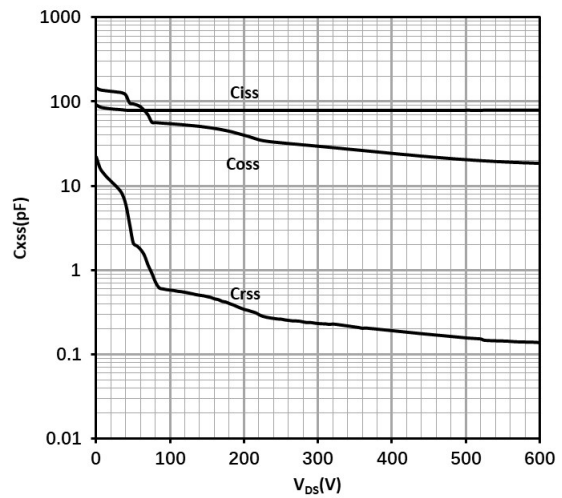
$I_D = f(V_{DS}); T_C = 125\text{ }^\circ\text{C}$

Figure 18 Typ. gate charge



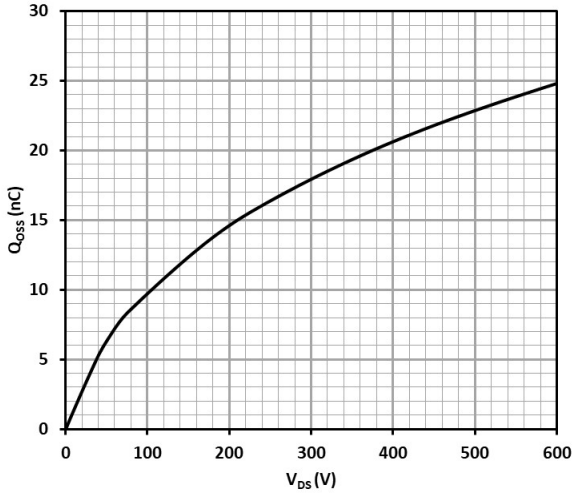
$V_{GS} = f(Q_G); V_{DCLINK} = 400\text{ V}; I_D = 3\text{ A}$

Figure 19 Typ. capacitances



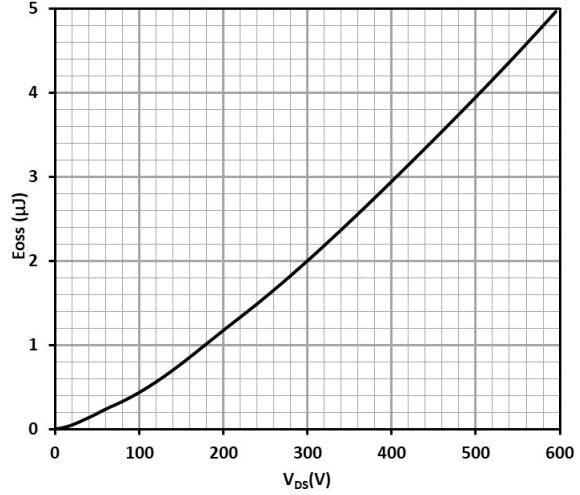
$C_{XSS} = f(V_{DS}); \text{Freq.} = 100\text{ kHz}$

Figure 20 Typ. output charge



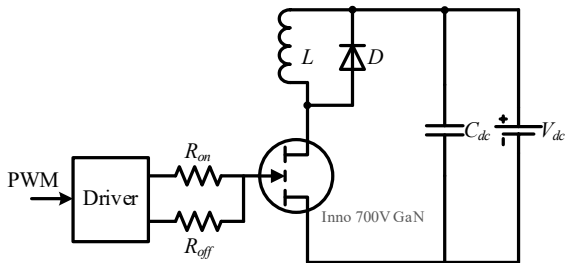
$Q_{oss} = f(V_{DS}); \text{Freq.} = 100 \text{ kHz}$

Figure 21 Typ. Coss stored Energy



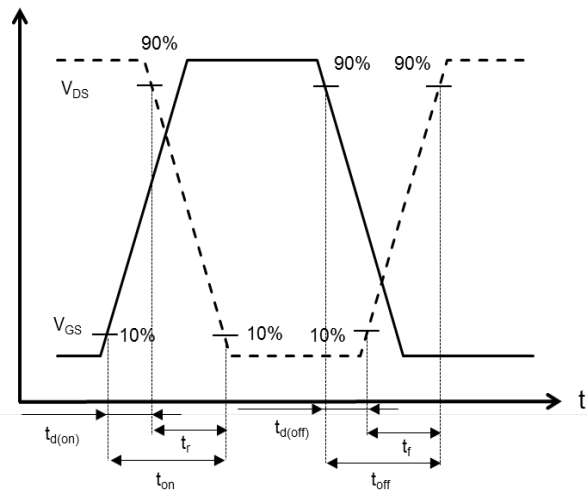
$E_{oss} = f(V_{DS}); \text{Freq.} = 100 \text{ kHz}$

Figure 22 Typ. Switching times with inductive load

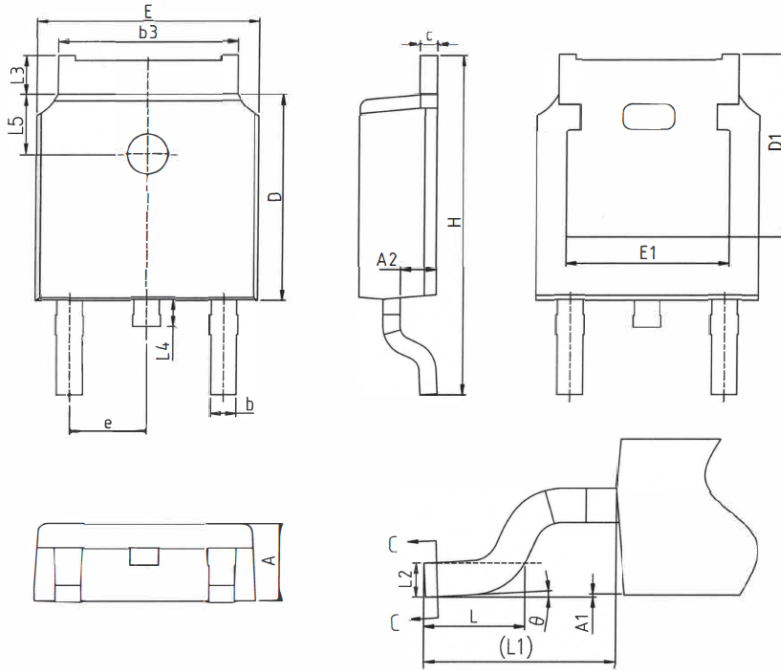


$V_{DS} = 400 \text{ V}, I_D = 6 \text{ A}, L = 318 \mu\text{H}, V_{GS} = 6 \text{ V},$
 $R_{on} = 10 \Omega, R_{off} = 2 \Omega$

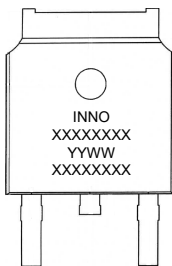
Figure 23 Typ. Switching times waveform



10. Package outlines



SYMBOL	MM			SYMBOL	MM		
	MIN	NOM	MAX		MIN	NOM	MAX
A	2.20	2.30	2.40	e	2.286BSC		
A1	0.00	-	0.13	H	9.40	10.10	10.50
A2	0.92	1.07	1.17	L	1.38	1.50	1.75
b	0.63	0.78	0.90	L1	2.90REF		
b3	5.10	5.33	5.46	L2	0.51BSC		
c	0.43	0.53	0.61	L3	0.88	-	1.28
D	5.98	6.10	6.22	L4	0.50	-	1.00
D1	5.30REF			L5	1.65	1.80	1.95
E	6.40	6.60	6.73	θ	0°	-	8°
E1	4.83REF						



ROW	Description	Example
Row1	Company name	INNO
Row2	Product code	XXXXXXXX
Row3	Date code	YYYY
Row4	ASSY lot No.	XXXXXXXX

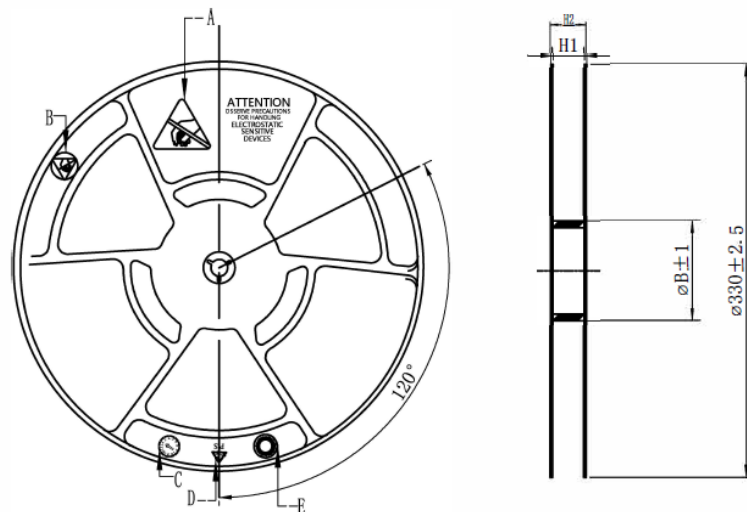
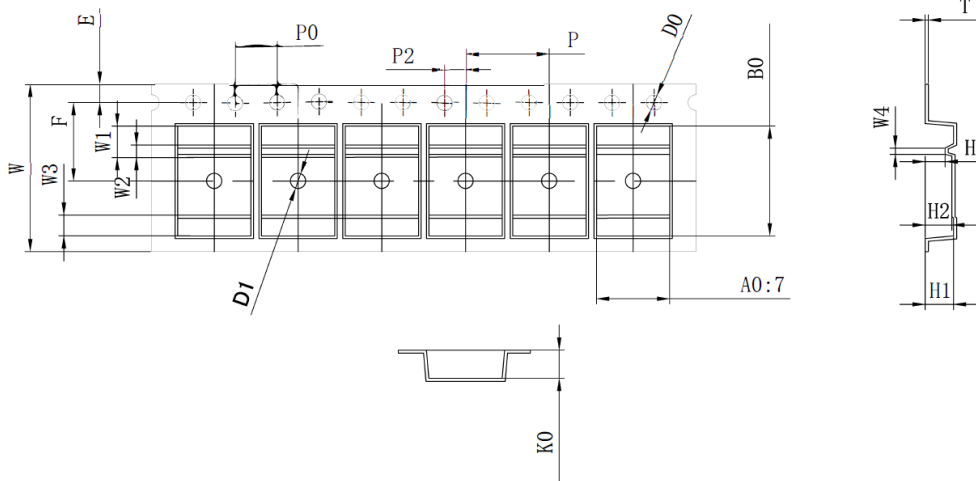
Notes:

- (1) All dimension are in millimeters.
- (2) Drawing is not to scale.
- (3) Dimensions do not include mold protrusion.
- (4) Package outline exclusive of metal burr dimensions.

11. Reel information

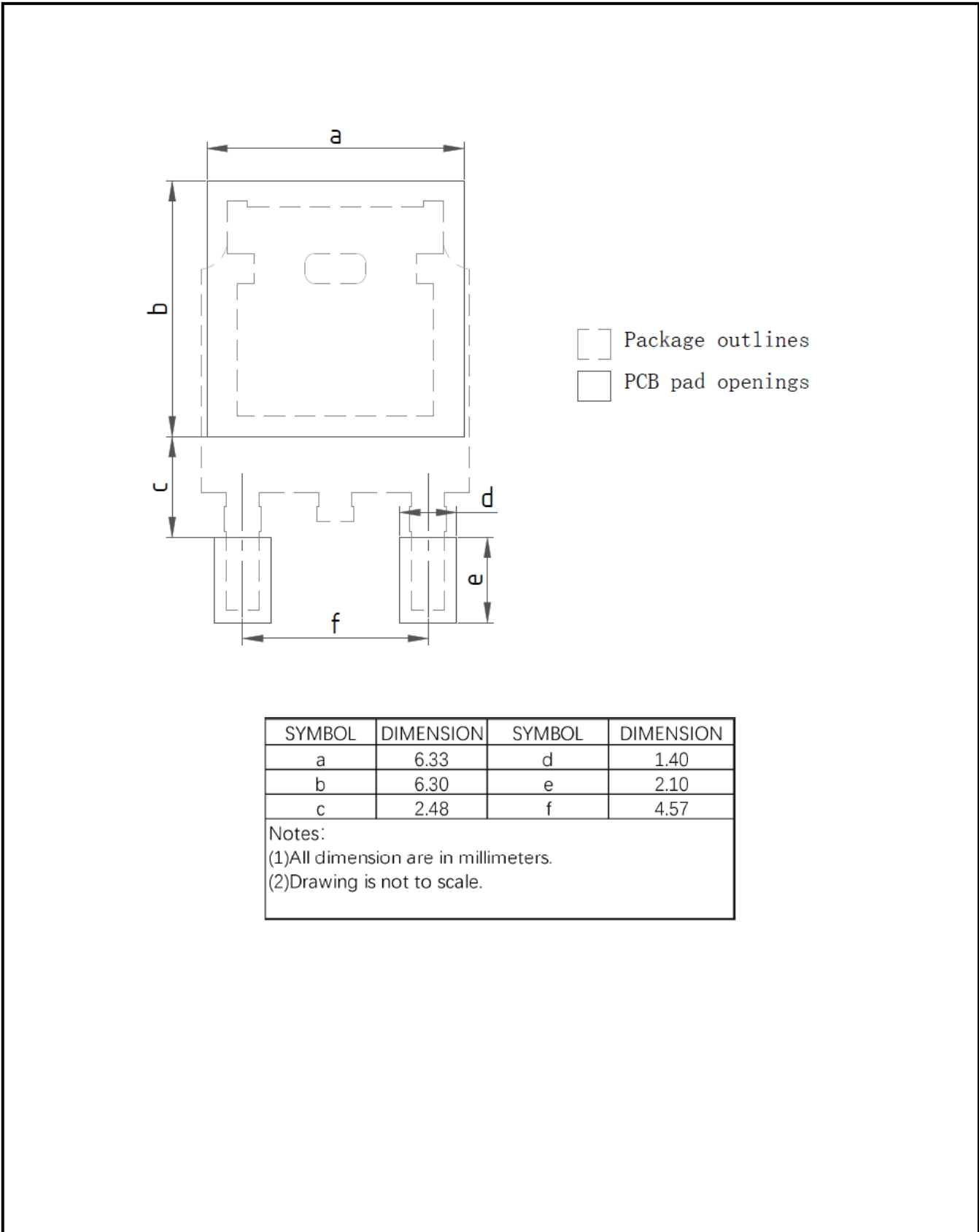
D	16.0	0.30	8.00	7.00	10.50	2.70	0.00	1.75	7.50	4.00	2.00	1.55	1.50	3.0	1.2	2.0	2.7	2.5	1.7	0.6
A	+0.40	+0.08	+0.15	+0.20	+0.15	+0.15	+0.00	+0.15	+0.15	+0.15	+0.15	+0.15	+0.25	+0.15	+0.15	+0.15	+0.15	+0.15	+0.15	+0.15
T	-0.20	-0.08	-0.15	-0.20	-0.15	-0.15	-0.10	-0.15	-0.15	-0.15	-0.15	-0.15	-0.25	-0.15	-0.15	-0.15	-0.15	-0.15	-0.15	-0.15
A	W	T	P	A0	B0	K0	K1	E	F	P0	P2	D0	D1	W1	W2	W3	H1	H2	H3	W4

Unit:mm



Unit:	mm
Tape Width	16
H1	16.4±0.1
H2MAX	22.4

12. Recommended PCB footprint



13. Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2023-07-20	1.0 version release
1.1	2023-12-26	1) Update Typ. channel reverse characteristics: add $V_{gs}=-6/-4V$ (Figure 5 & Figure 6) 2) Add Reel information

Important Notice

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